

## Notice of References Cited

Applicant/Patent  
Sutera et al.

Application/Control No.  
09/430,350

Examiner  
Hugh Jones

Art Unit  
2123

Page 1 of 2

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	Document Number Country Code-Number-Kind Code	Date MM-YYYY <sup>1</sup>	Name	Classification <sup>2</sup>	
A	5,666,288	9/1997	Jones et al.	716	17
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O					
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R					
S					
T					

### NON-PATENT DOCUMENTS

	Include, as applicable: Author, Title, Date, Publisher, Edition or Volume, Pertinent Pages
u	Lillis et al.: "Optimal wire sizing and buffer insertion for low power and a generalized delay model"; IEEE; pp. 437-447; 3/1996.
v	Dhar et al.; "Optimum buffer circuits for driving long uniform lines"; IEEE J. Solid State Ckts; pp. 32-40; 1/1991.
w	Alpert et al.; "Buffer insertion for noise and delay optimization"; IEEE Proc. 98 Design Automation Conf.; pp. 362-367; 6/1998.
x	Culetu et al.; "A practical repeater insertion method in high speed VLSI circuits"; IEEE 98 Design Automation Conf.; pp. 392-395; 6/1998.

<sup>1</sup> A copy of this reference is not being furnished with this Office action. See MPEP § 707.05(a).

<sup>1</sup> Dates in MM-YYYY format are publication dates.

<sup>2</sup> Classifications may be U.S. or foreign.

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